REMARKS

In response to the Official Action mailed March 29, 2002, Applicants amend their application and request reconsideration. In this Amendment, no claims are added and claims 3 and 4 are canceled so that claims 1, 2, and 5-8 remain pending. Claim 9 is not being examined pursuant to a restriction requirement and election.

Changes are made to the specification to conform the specification to the description to Figure 1.

The invention relates to a high frequency power amplifier, which comprises a transistor and an impedance matching circuit on the input side of the transistor. The impedance matching circuit effectively increases the reflection of higher harmonics, thus improving the efficiency of the transistor. The invention achieves this reflection without limiting the input-side higher harmonic load of the impedance matching circuit to that of a short circuit load.

In this Amendment, claims 1 and 3 are combined as amended claim 1. In view of the identity of the limitations of claims 3 and 4, this combination requires the cancellation of claims 3 and 4. In view of this Amendment, the only pertinent rejections are those pertaining to claims 2, 3, and 5-8.

Claims 1-8 are rejected as unpatentable over Kato et al. (U.S. Pat. No. 6,262,641, hereinafter Kato). Applicants respectfully traverse the rejection.

According to the Official Action, all examined claims are obvious over Figure 1 of Kato. Applicants respectfully disagree.

The Examiner rejected claim 3 by asserting that a third harmonic reflecting circuit, a second harmonic processing circuit, and a fundamental wave matching circuit, are inherent in Kato. However, the Official Action provides no rationale or evidence supporting a rejection based on inherency. Where is the third harmonic reflecting circuit in Kato? In order to demonstrate that this and the other limitations of claim 3 are inherent in Kato, the Examiner must establish that those limitations **necessarily** occur in Kato. Clearly, they do not. This rejection must be withdrawn as to amended claim 1 and its dependent claim 2.

There is a substantial difference in function and structure between the invention and Kato. Kato is directed to a frequency multiplier, i.e., a circuit that produces an output signal having a frequency higher than the frequency of the input signal by an integer factor. Normally, at the input side of the frequency multiplier, an open circuit load is employed to reflect frequencies other than the fundamental frequency that is to be multiplied in the frequency multiplier.

By contrast, it is not normal to employ an open circuit load in the input side of a power amplifier with respect to any harmonics of a fundamental wave of an input signal that is to be amplified by the amplifier. Rather, in the past, as explained in the patent application at page 1, lines 22-30, it has been believed that supplying a short circuit load at the input side of a power amplifier is the appropriate step for increasing efficiency of the amplifier. This information is provided, for example, in the Japanese patent cited in that passage, which corresponds to U.S. Patent 5,592,122, a copy of which is enclosed with the accompanying Information Disclosure Statement. Attention is directed to Figures 5 and 6 of that U.S. Patent 5,592,122 and particularly to its Figures 5 and 6 and the passages at column 3, lines 25-29 and column 6, lines 33-55.

Contrary to the prior art, the invention provides a substantially open circuit load with respect to even number higher harmonics of an input signal and including a third harmonic reflecting circuit in the power amplifier of claim 1. The power amplifier of claim 5 includes an input-side impedance matching circuit that functions as a substantially short-circuit load with respect to odd number harmonics of the input signal. These structures are based upon the inventors' investigations and the measurements illustrated in Figure 2 of the patent application, none of which is disclosed nor suggested by Kato. Therefore, a person of skill in the art would not, from either Kato or U.S. Patent 5,592,122, considered separately or even in combination, find a suggestion for the invention as defined by the claims now pending.

Claim 5 is an independent claim describing a high frequency power transistor having an input-side impedance matching circuit that provides a substantially short circuit load to odd number harmonics as to a wave at a fundamental frequency. In rejecting all claims, the Examiner misstated a basic tenet of transmission line technology. According to the Examiner, it "is well known [that] a short or open is required for reflections." This statement is incorrect. An impedance mismatch in transmission lines is very well known to produce reflections. Further, the Examiner stated that it would have been obvious to have adjusted the length and width of transmission lines to specific dimensions to achieve desired load conditions. This statement is correct. However, the statement does not furnish a basis for modifying Kato in any way that could produce the claimed invention. How is it known what load conditions are desired? Only knowledge of the invention could provide that information. That knowledge cannot be relied upon to reject the claims. Moreover, even if the desired load condition is known, there are multiple ways of achieving that condition. How does one select among those ways to suggest the invention? The conclusion is that general principles of technology do not point in the direction of any particular structure, and certainly not the structure of claim 5.

In that structure, the input-side impedance matching circuit provides a short circuit load to odd number harmonics. There is no such element nor the equivalent of such an element in Figure 1 of Kato. The only potentially corresponding element in Kato is the stub 3 that provides reflection of second harmonic signals generated in the FET and reflects those signals back to the FET. Second harmonics are not odd number harmonics and there is no element in Figure 1 of Kato that deals with odd number harmonics, much less provides a substantially short circuit load to odd harmonics. The part of claim 5 missing from Kato, a difference acknowledged to be present because the rejection is for obviousness and not for anticipation, is simply not supplied by general principles of transmission line technology. Thus, the rejection of claims 5-8 cannot be maintained and must be withdrawn.

With regard to claims 7 and 8, the limitations of those claims were dismissed as inherent, just as the limitation of claim 3 was dismissed. This rejection is respectfully traversed for the same reasons already expressed with respect to the rejection of former claim 3, now amended claim 1. The Examiner has not carried his burden with respect to an inherency rejection because he has not demonstrated that the three separately identified elements of claims 7 and 8 are, in fact, present in Figure 1 of Kato, but not identified by reference number or description. The rejection of these claims should be withdrawn.

Applicants note that claims 2 and 6 have been rejected as optimizations. Applicants respectfully disagree. However, since those claims depend from claims that are patentable over the only reference applied in rejecting the claims, for the reasons already supplied, the rejections of claims 2 and 6 do not need further comment.

Reconsideration and withdrawal of the rejection, as well as allowance of the pending and examined claims, are appropriate and earnestly solicited.

Respectfully submitted,

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PATENT
Attorney Docket No. 401256/Takada

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

GOTOU et al.

Application No. 09/881,665 Art Unit: 2817

Filed: June 18, 2001 Examiner: H. Choe

For: HIGH FREQUENCY POWER AMPLIFIER

AMENDMENTS TO SPECIFICATION AND CLAIMS MADE IN RESPONSE TO OFFICE ACTION DATED MARCH 29, 2002

Amendments to the paragraph beginning at page 4, line 32:

Fig. 1 shows a circuit configuration of a high frequency power amplifier ~~in~~ as a First Embodiment of the present invention. In Fig. 1, reference numeral 1 denotes a transistor, 2 denotes a first signal line ~~1~~ (line length: L1, line width: W1), 3 denotes a second signal line ~~2~~ (line length: L2, line width: W2), 4 denotes a third signal line ~~3~~ (line length: L3, line width: W3), 5 denotes a fourth signal line ~~4~~ (line length: L4, line width: W4), 6 denotes a fifth signal line ~~5~~ (line length: L5, line width: W5), 7 denotes an output-side matching circuit, 8 denotes a signal input terminal, and 9 denotes a signal output terminal. If impedance is not matched in the middle or ends of signal lines ~~1~~ 2-6 or the like, a part of the incident wave is reflected. The ratio of this reflected wave to the incident wave is called a reflection coefficient. In Fig. 1, reference numeral 10 denotes the reflection coefficient (Γin) when the input-side matching circuit is viewed from the direction of the transistor 1. In general, the voltage V(z) in the z-direction of the signal line that has a phase constant of β is represented by the following Equation 1.

Amendments to the paragraph beginning at page 5, line 25:

As Fig. 1 shows, signal lines ~~3,~~ 4, 5, and ~~5~~ 6 are connected in series, the signal line ~~1~~ 2 is connected to the node A between signal lines ~~3~~ 4 and ~~4~~ 5, and the signal line ~~2~~ 3 is connected to the node B between signal lines ~~4~~ 5 and ~~5~~ 6. By adjusting line lengths L1 to L5 and line widths W1 to W5 of the signal lines ~~1~~ 2 to ~~5~~ 6 shown in Fig. 1, the 2nd ~~higher~~ harmonic is adjusted to be an open load (the reflected phase angle of Γin: 0 – 90°, the

quantity of reflection: 0.6 – 1.0), and the 3rd ~~higher~~ harmonic is adjusted to ~~be~~ have a short-circuit load (the reflected phase angle of Γin: 110 – 270°, the quantity of reflection: 0.6 – 1.0).

Amendments to the paragraph beginning at page 6, line 14:

According to the First Embodiment, as described above, by adjusting line lengths L1 to L5 and line widths W1 to W5 of the signal lines ~~1~~ 2 to ~~5~~ 6 in a high frequency power amplifying circuit shown in Fig. 1, the 2nd ~~higher~~ harmonic can be adjusted to be an open load (the reflected phase angle of Γin: 0 – 90°, the quantity of reflection: 0.6 – 1.0), and the 3rd ~~higher~~ harmonic is adjusted to be short-circuit load (the reflected phase angle of Γin: 110 – 270°, the quantity of reflection: 0.6 – 1.0). Therefore, by optimizing the input-side ~~higher~~ harmonic load of the impedance-matching circuit, the efficiency of transistor operation can be improved.

Amendments to existing claims:

Cancel claims 3 and 4.

1. (Twice Amended) A high frequency power amplifier, comprising:

a transistor for amplifying signals and having an input side; and

an input-side impedance matching circuit connected ~~to an~~ between the input side of said transistor and a signal input terminal of the amplifier, wherein said input-side impedance matching circuit provides an impedance of a substantially open circuit load with respect to even number higher harmonics of a fundamental wave of a high frequency signal and comprises a third harmonic reflecting circuit, a second harmonic processing circuit, and a fundamental wave matching circuit, disposed sequentially from the signal input terminal.

5. (Twice Amended) A high frequency power amplifier, comprising:

a transistor for amplifying signals and having an input side; and

an input-side impedance matching circuit connected ~~to an~~ between the input side of said transistor and a signal input terminal of the amplifier, wherein said input-side impedance matching circuit provides an impedance of a substantially short-circuit load with respect to odd number harmonics of a fundamental wave of a high frequency signal.

7. (Twice Amended) The high frequency power amplifier according to claim 6, wherein said input-side impedance matching circuit comprises a third harmonic reflecting circuit, a second harmonic processing circuit, and a fundamental wave matching circuit, disposed sequentially from ~~a~~ the signal input terminal.

8. (Twice Amended) The high frequency power amplifier according to claim 5, wherein said input-side impedance matching circuit comprises a third harmonic reflecting circuit, a second harmonic processing circuit, and a fundamental wave matching circuit, disposed sequentially from ~~a~~ the signal input terminal.